Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	858	(fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:02
L2	228	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and map$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:03
L3	153	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and map$4 and address and configur$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:04
L4	35	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and map$4 and address and configur$4 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:35
L5	148	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and map$4 and address and configur$4 and stor$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:38
L6	125	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and map$4 and address and configur$4 and stor$3 and register	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:40
L7	54	((fpga or field adj programmable adj gate adj array) same (clb or configurable adj logic adj block) same function) and (map$4 same address) and configur$4 and stor$3 and register	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 14:40

	Document ID	Title	Current OR
1	US 20040216074 A1	Structures and methods for selectively applying a well bias to portions of a programmable device	716/16
2	US 20040088671 A1	Adaptive adjustment of constraints during PLD placement processing	716/16
3	US 20040060032 A1	Automated system for designing and developing field programmable gate arrays	716/16
4	US 20040025135 A1	Structures and methods for selectively applying a well bias to portions of a programmable device	716/16
5	US 20040010767 A1	Hierarchical general interconnect architecture for high density fpga's	716/16
6	US 20030172364 A1	Software programmable multiple function integrated circuit module	716/17
7	US 20030121010 A1	System, method, and article of manufacture for estimating a potential performance of a codesign from an executable specification	716/4
8	US 20020010902 A1	Field programmable gate array (FPGA) bit stream cormat	716/16
9	US 6839888 B2	Method for implementing bit-swap functions in a field programmable gate array	716/16
10	US 6836842 B1	Method of partial reconfiguration of a PLD in which only updated portions of configuration data are selected for reconfiguring the PLD	713/100
11	US 6785873 B1	Emulation system with multiple asynchronous clocks	716/4

	Document ID	Title	Current OR
12	US 6777978 B2	Structures and methods for selectively applying a well bias to portions of a programmable device	326/38
13	US 6772405 B1	Insertable block tile for interconnecting to a device embedded in an integrated circuit	716/11
14	US 6772230 B2	Field programmable gate array (FPGA) bit stream format	710/8
15	US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language capable of programming hardware architectures	717/114
16	US 6651225 B1	Dynamic evaluation logic system and method	716/4
17	US 6624654 B1	Methods for implementing circuits in programmable logic devices to minimize the effects of single event upsets	326/14
18	US 6487648 B1	SDRAM controller implemented in a PLD	711/167
19	US 6408422 B1	Method for remapping logic modules to resources of a programmable gate array	716/3
20	US 6389379 B1	Converification system and method	703/14
21	US 6370677 B1	Method and system for maintaining hierarchy throughout the integrated circuit design process	716/8
22	US 6321366 B1	Timing-insensitive glitch-free logic system and method	716/6

	Document ID	Title	Current OR
23	US 6216257 B1	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	716/16
24	US 6205574 B1	Method and system for generating a programming bitstream including identification bits	716/16
25	US 6035106 A	Method and system for maintaining hierarchy throughout the integrated circuit design process	703/1
26	US 5870309 A	HDL design entry with annotated timing	716/6
27	US 5838954 A	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/16
28	US 5825662 A	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/3
29	US 5761483 A	Optimizing and operating a time multiplexed programmable logic device	716/2
30	US 5701441 A	Computer-implemented method of optimizing a design in a time multiplexed programmable logic device	716/16
31	US 5526278 A	Method and apparatus for converting field-programmable gate array implementations into mask-programmable logic cell implementations	716/16
32	US 5521837 A	Timing driven method for laying out a user's circuit onto a programmable integrated circuit device	716/10

	Document ID	Title	Current OR
33	US 5513124 A	Logic placement using positionally asymmetrical partitioning method	716/7
34	US 5448496 A	Partial crossbar interconnect architecture for reconfigurably connecting multiple reprogrammable logic devices in a logic emulation system	716/16
35	US 5224056 A	Logic placement using positionally asymmetrical partitioning algorithm	716/7